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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 09/990,274  | 11/23/2001  | Chun-Yang Hsiao      | MR2707-3            | 2402             |
| 4586  | 7590        | 01/12/2005           | EXAMINER            |                  |
| ROSENBERG, KLEIN & LEE<br>3458 ELLICOTT CENTER DRIVE-SUITE 101<br>ELLICOTT CITY, MD 21043 |             |                      | KIM, DAVID S        |                  |
|   |             |                      | ART UNIT            | PAPER NUMBER     |
|   |             |                      | 2633                |                  |

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/990,274

Applicant(s)

HSIAO, CHUN-YANG

Examiner

David S. Kim

Art Unit

2633

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 23 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities:

On p. 5, l. 11, "FIG. 1" is used where -- FIG. 3 -- may be intended.

On p. 6-7, bridging paragraph, the following sentence reads awkwardly, "When an infrared signal of ultrasonic signal is detected *and under the circumstances of the reset period t of the fixed-interval reset circuit 38 is greater than the period of the carrier signal for infrared or ultrasonic transmission*, the unmodulated or original signal will be fetched and outputted and the influence of the duty cycle is avoided." In particular, the italicized portion appears to lack a subject.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-3** are rejected under 35 U.S.C. 102(b) as being anticipated by Ichikawa et al. (U.S. Patent No. 5,684,830, hereinafter "Ichikawa").

**Regarding claim 1**, Ichikawa discloses:

An integrated circuit receiver available for infrared or ultrasonic transmission with digital filtering comprising:

an infrared receiver (photodiode 341 in Fig. 29; photodiode 13 in Fig. 2) or ultrasonic transducer for receiving a transmitted signal from outside of said integrated circuit receiver and producing a carrier signal;

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an amplifier (amplifier 342 in Fig. 29; amplifier 14 in Fig. 2) connected to said infrared receiver or ultrasonic transducer for amplifying said carrier signal to be an amplified signal; and  
a digital filter (digital circuit section 350 in Fig. 29; digital section 12 in Fig. 2) connected to said amplifier for filtering out a carrier component from said amplified signal to recover an original signal.

**Regarding claim 2, Ichikawa discloses:**

An integrated circuit receiver according to claim 1 wherein said digital filter comprising:  
a fixed-interval reset circuit (circuitry 352-354 in Figs. 29 and 31; circuitry 42-43 in Fig. 5) connected to said amplified signal for producing a fetched signal; and  
a fixed-interval sample circuit (demodulating section 355 in Figs. 29 and 31; demodulating section 46 in Fig. 5) connected to said fixed-interval reset circuit for demodulating said fetched signal.

**Regarding claim 3, Ichikawa discloses:**

An integrated circuit receiver according to claim 2 wherein said fixed-interval reset circuit and fixed-interval sample circuit are constructed with flip-flops (note flip-flops in Fig. 31; note flip-flops in Fig. 5).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ichikawa.

**Regarding claim 4, Ichikawa discloses:**

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An integrated circuit receiver according to claim 2 wherein said fixed-interval reset circuit and fixed-interval sample circuit are triggered on a rising edge (note flip-flops with uninverted inputs to their clock input ports in Figs. 5, 14, 17-20, and 31) and falling edge (note flip-flops with inverted inputs to their clock input ports in Figs. 5, 14, and 31) of a clock.

Ichikawa does not expressly disclose:

An integrated circuit receiver according to claim 2 wherein said fixed-interval reset circuit and fixed-interval sample circuit are triggered on a rising edge and falling edge of a clock, *respectively*.

Rather, in some examples, Ichikawa shows said fixed-interval reset circuit being triggered on a *falling* edge (e.g., flip-flops of circuitry 352-354 in Fig 31 with inverted inputs to their clock input ports; flip-flops of circuitry 42-43 in Fig. 5 with inverted inputs to their clock input ports) and said fixed-interval sample circuit being triggered on a *rising* edge (e.g., flip-flops of circuitry 352-354 in Fig 31 with uninverted inputs to their clock input ports; flip-flops of circuitry 42-43 in Fig. 5 with uninverted inputs to their clock input ports) of a clock, *which is the reverse of the edge triggering logic of the claim limitation introduced by claim 4*. However, reversing the logic of a digital system is an extremely well known practice in the art. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to reverse the edge triggering logic of the digital system of Ichikawa. One of ordinary skill in the art would have been motivated to do this since it is a conventional way to provide a design alternative that also maintains the main functionality of the digital system.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Liu et al. is cited to show a digital circuit that comprises one circuit triggered on a rising edge and another circuit triggered on a falling edge.

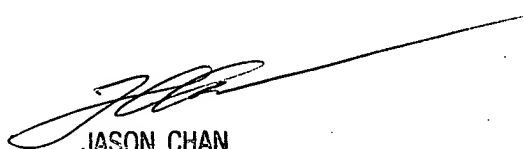
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Kim whose telephone number is 571-272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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